Listing of Claims:

13. (Currently Amended) A method for selecting a clock signal from a plurality of parallel clock signals received from a plurality of parallel transmission paths in a digital data transmission, comprising the steps of:

receiving, at a unit comprising a changeover device, parallel clock signals from at least two parallel transmission paths, the parallel ~~clock~~ clock signals being generated from a single originating signal, a first clock signal of the parallel clock signals being designated the selected clock signal and being transmitted to an output of the unit;

requesting, by the changeover device, a change of the selected clock signal from the first clock signal to a second clock signal of the parallel clock signals based on an indication received from a phase locked loop of an unreliability in locking the first clock signal;

determining whether the first and second clock signals are both in a predetermined mode and determining whether a polarity of a signal phase difference of the first and second clock signals is inverted, thereby indicating the same phase or a phase shift of 180°;

generating a first signal when it is determined that the first and second clock signals are in the predetermined mode, initiating a time delay when it is determined that ~~the selected clock signal to the second clock signal that~~ the polarity of the signal phase difference of the first and second clock signals is inverted, and generating a second signal after the time delay has elapsed; and

changing the selected clock signal to the second clock signal in response to said step of requesting and when said first and second signals are present, whereby said step of changing occurs proximate a phase coincidence of the first and second clock signals.

14. (Previously Prevented) The method of claim 13, wherein said step of requesting comprises requesting the changing of the selected clock signal using a control signal generated

by the changeover device, the control signal being based on the indication of an unreliability of the locking of the first clock signal by a lock loop; and wherein said step of changing comprises regulating a multiplexer to change the clock signals when the control signal, the first signal, and the second signal are present.

15. (Currently Amended) A unit for digital data transmission and for changing parallel clock signals in the digital data transmission, comprising:

a changeover device including means for receiving parallel clock signals from at least two parallel data transmission paths, the parallel clock signals being generated from a single originating clock signal;

means for forwarding a selected one of the parallel clock signals to an output of the unit; and

means for changing a selected clock signal from a first clock signal of the parallel clock signals to a second clock signal of the parallel clock signals based on an indication of unreliability of locking the selected clock signal;

means for detecting whether the first and second clock signals are in an identical mode and that a polarity of a signal phase difference is inverted;

wherein the change of the selected clock signal occurs after a delay to ensure that the changeover occurs while the clock signals are static.

16. (Previously Prevented) The unit of claim 15, wherein said changeover device comprises an application specific integrated circuit including:

a clock signal multiplexer having means for determining when a suitable clock signal phase is present and means for performing the change of the selected clock signal when the suitable clock signal phase is present;

at least two data frame decoding blocks for respectively receiving the parallel clock signals and associated data signals from the at least two data transmission paths and forming decoded control signals and data signals therefrom;

at least two elastic buffer and control blocks receiving the decoded control signals and decoded data signals and forming data signals that are synchronized by the selected clock signal;

a data signal multiplexer selecting the data signal to be received; and

a further decoding block synchronizing the received data signal using the selected clock signal into a final data signal and controlling the data signal multiplexer using a synchronizing signal generated by said at least two data frame decoding blocks.

17. (Previously Prevented) The unit of claim 15, wherein the unit is part of a radio link in a mobile telecommunications system.

18. (Canceled)

19. (Canceled)

20. (Previously Prevented) An arrangement for digital data transmission, comprising:

a first indoor unit for dividing a clock signal to be transmitted into parallel clock signals;

a second indoor unit for receiving the parallel clock signals, selecting one of the parallel clock signals as a selected clock signal, and transmitting the selected clock signal to an output of the selected clock signal;

a first changeover device in said first indoor unit and a second changeover device in said second indoor unit for receiving the parallel clock signals; and

first and second outdoor units each provided with a transmitter for transmitting one of the parallel clock signals to be changed and respectively a receiver for receiving a parallel clock signal, and a phase lock synchronized with the selected clock signal, said second changeover device generating a request for changing the selected clock signal from a first clock signal to a second clock

signal of the parallel clock signals based on an indication of an unreliability in locking the selected clock signal with the phase lock.

21. (Previously Prevented) The arrangement of claim 20, wherein each of said first and second changeover devices is realized in an application specific integrated circuit which comprises:

a clock signal multiplexer having means for determining when a suitable clock signal phase is present and means for performing the changeover when the suitable clock signal phase is present;

at least two data frame decoding blocks for respectively receiving the parallel clock signals and associated data signals from the at least two data transmission paths and forming decoded control signals and data signals therefrom;

at least two elastic buffer and control blocks respectively receiving the decoded control signals and decoded data signals and forming data signals that are synchronized by the selected clock signal;

a data signal multiplexer selecting the data signal to be received; and

a further decoding block synchronizing the received data signal using the selected clock signal into a final data signal and controlling the data signal multiplexer using a control signal generated by said at least two data frame decoding blocks.

22. (Previously Prevented) The arrangement of claim 21, wherein the control signal includes a synchronizing signal, a bit error signal, a frame alignment alarm signal, and a pseudo frame signal.

23. (Previously Prevented) The arrangement of claim 21, wherein said clock signal multiplexer comprises:

a first block for detecting identical modes of the parallel clock signals, said first block generating an active signal when the parallel clock signals are in the same mode;

D-flip-flop circuits forming a phase shift sensitive coupling;

a second block for detecting un-identical modes of the clock signals connected to outputs of the phase shift sensitive coupling, an output of said second block being raised, in response to said phase shift sensitive coupling, to the value one after a period of one cycle of the second parallel clock signal has passed from the moment when the polarity of the phase difference between the parallel clock signals was changed;

a delay circuit for delaying the output signal from said second block;

a third block checking for the request for changing the selected clock signal, the output signal from the first block, and the delayed output signal from the second block; and

a multiplexer for changing the selected clock signal from the first clock signal to the second clock signal under the control of said third block when the request for change, the output signal from the first block, and the delayed output signal from the second block are present at the third block.

24. (Previously Prevented) A changeover device for selecting a clock signal from a plurality of parallel clock signals, comprising:

means for receiving parallel clock signals from at least two data transmission paths, the parallel clock signals being generated from a single originating clock signal, and selected a selected clock signal from the parallel clock signals;

means for receiving a control signal indicating an unreliability of locking the selected clock signal;

change requirement means for determining a change in the selected clock signal is required from a first clock signal to a second clock signal in response to the control signal;

same mode means for determining that the first and second clock signals are in the same mode;

inversion means for determining an inversion of the polarity of the signal phase difference between the first and second clock signals indicating a situation, thereby indicating that the first and second signals were either in the same phase or in a phase shift of 180°; and

control means for checking said change requirement means, said same mode means, and said inversion means, initiating a time delay when a requirement for a change is determined, the first and second clock signals are in the same mode, and the inversion is determined, and performing the changeover after the time delay is elapsed to ensure that the changeover is effected while the clock signals are in a static mode.

25. (Previously Prevented) An application specific integrated circuit, comprising:

means for receiving parallel clock signals from at least two data transmission paths, the parallel clock signals being generated from a signal originating clock signal, and selected a selected clock signal from the parallel clock signals;

means for receiving a control signal indicating an unreliability of locking the selected clock signal;

change requirement means for determining a change in the selected clock signal is required from a first clock signal to a second clock signal in response to the control signal;

same mode means for determining that the first and second clock signals are in the same mode;

inversion means for determining an inversion of the polarity of the signal phase difference between the first and second clock signals indicating a situation, thereby indicating that the first and second signals were either in the same phase or in a phase shift of 180°; and

control means for checking said change requirement means, said same mode means, and said inversion means, initiating a time delay when a requirement for a change is determined, the first and second clock signals are in the same mode, and the inversion is determined, and performing the changeover after the time delay is elapsed to ensure that the changeover is effected while the clock signals are in a static mode.

26. (Previously Prevented) A clock multiplexer, comprising:

means for receiving first and second parallel clock signals from two data transmission paths, the first and second parallel clock signals being generated from a signal originating clock signal, said first parallel clock signal being a selected clock signal;

a first block generating an active signal when the parallel clock signals are in the same mode;

D-flip-flop circuits forming a phase shift sensitive coupling;

a second block detecting un-identical modes of the clock signals connected to outputs of the phase shift sensitive coupling, an output of said second block being raised, in response to said phase shift sensitive coupling, to the value one after a period of one cycle of the second parallel clock signal has passed from a point in time when the polarity of the phase difference between the parallel clock signals was changed;

a delay circuit for delaying the output signal from said second block;

a third block checking for the request for changing the selected clock signal, the output signal from the first block, and the delayed output signal from the second block; and

a multiplexer for changing the selected clock signal from the first clock signal to the second clock signal under the control of said third block when the request for change, the output signal from the first block, and the delayed output signal from the second block are present at the third block.

27. (Previously Prevented) An application specific integrated circuit, comprising:

means for receiving first and second parallel clock signals from two data transmission paths, the first and second parallel clock signals being generated from a signal originating clock signal, said first parallel clock signal being a selected clock signal;

a first block generating an active signal when the parallel clock signals are in the same mode;

D-flip-flop circuits forming a phase shift sensitive coupling;

a second block detecting un-identical modes of the clock signals connected to outputs of the phase shift sensitive coupling, an output of said second block being raised, in response to said phase shift sensitive coupling, to the value one after a period of one cycle of the second parallel clock signal has passed from a point in time when the polarity of the phase difference between the parallel clock signals was changed;

a delay circuit for delaying the output signal from said second block;

a third block checking for the request for changing the selected clock signal, the output signal from the first block, and the delayed output signal from the second block; and

a multiplexer for changing the selected clock signal from the first clock signal to the second clock signal under the control of said third block when the request for change, the output signal from the first block, and the delayed output signal from the second block are present at the third block.